Amendments to the Claims

Claim 1 (previously presented): A method of forming a transistor device, comprising:

providing a silicon-comprising surface;

exposing the silicon-comprising surface to activated nitrogen to form a peak nitrogen concentration within the silicon-comprising surface of at least 15% (atom percent), the exposing forming a material comprising silicon and nitrogen;

providing a channel region on one side of the material comprising silicon and nitrogen;

providing a transistor gate structure on a side of the material comprising silicon and nitrogen that is opposed to said one side; and

forming a pair of source/drain regions separated from one another by the channel region.

Claim 2 (original): The method of claim 1 further comprising forming a layer of silicon dioxide over the channel region, and wherein the silicon-comprising surface is a surface of the silicon dioxide.

Claim 3 (original): The method of claim 1 wherein the transistor device is a PMOS device.

Claim 4 (original): The method of claim 1 wherein the transistor device is an NMOS device.

Claim 5 (original): The method of claim 1 further comprising subjecting the material comprising silicon and nitrogen to an anneal at a temperature of about 900°C for a time of from about 10 seconds to about 60 seconds; and wherein the material comprising silicon and nitrogen is heated to the anneal temperature by rapid thermal processing at a temperature ramp rate of at least about 10°C/second.

Claims 6-25 (cancelled).

Claim 26 (presently presented): A method of forming a transistor device, comprising:

providing a silicon-comprising material;

defining a channel region of the transistor device beneath the silicon-comprising material;

implanting a dopant into the channel region to a concentration of less than about 7×10^{17} atoms/cm^3 as a V_t implant;

forming a dielectric material over the channel region; the forming of the dielectric material comprising exposing the silicon-comprising material to activated nitrogen to form a peak nitrogen concentration within the exposed silicon-comprising material of at least about 15 atom percent, the dielectric material comprising the exposed silicon-comprising material;

forming a transistor gate structure over the nitrogen-comprising material; and

forming a pair of source/drain regions separated from one another by the channel region.

Claim 27 (original): The method of claim 26 further comprising forming a layer of silicon dioxide over the channel region, and wherein the silicon-comprising material is the silicon dioxide.

Claim 28 (original): The method of claim 26 wherein the transistor device is a PMOS device.

Claim 29 (original): The method of claim 26 wherein the concentration of dopant in the V_t implant is less than 7×10^{17} atoms/cm^3.

Claim 30 (original): The method of claim 26 wherein the concentration of dopant in the V_t implant is from about 1×10^{17} atoms/cm^3 to 7×10^{17} atoms/cm^3.

Claim 31 (original): The method of claim 26 wherein the concentration of dopant in the V_t implant is from about 1×10^{17} atoms/cm^3 to 5×10^{17} atoms/cm^3.

Claim 32 (original): The method of claim 26 wherein the activated nitrogen is formed from a plasma maintained at a power of from about 1,500 watts to about 5,000 watts.

Claim 33 (original): The method of claim 26 wherein the activated nitrogen is formed from a plasma that is remote relative to the silicon-comprising material.

Claim 34 (original): The method of claim 26 wherein the activated nitrogen is formed from a plasma that contacts the silicon-comprising material.

Claim 35 (original): The method of claim 26 further comprising maintaining the silicon-comprising material at a temperature of from about 25°C to about 400°C during the exposing of the material to the activated nitrogen.

Claims 36-60 (cancelled).

Claim 61 (previously presented): A method of forming a plurality of transistor devices comprising:

providing a substrate having a surface, the surface comprising silicon;

incorporating at least 15% (atom percent) nitrogen into the surface by exposing the surface to activated nitrogen;

forming a pair of source/drain regions within the substrate, the pair of source/drain regions being separated from one another by a channel region, wherein each of the source/drain regions comprises a heavily doped portion proximate the channel region and a lightly doped portion separated from the channel region by the heavily doped portion; and

providing a transistor gate structure over both the surface and the channel region.

Claim 62 (previously presented): The method of claim 61 wherein the surface consists essentially silicon.

Claim 63 (previously presented): The method of claim 61 wherein the surface consists of silicon.

Claim 64 (previously presented): The method of claim 61 wherein the incorporating comprises forming the activated nitrogen by exposing a nitrogen precursor to a plasma.

Claim 65 (previously presented): The method of claim 61 wherein the surface has a thickness of less than 10 Å.

Claim 66 (previously presented): The method of claim 61 wherein the transistor device is a PMOS device.

Claim 67 (previously presented): The method of claim 61 wherein the transistor device is an NMOS device.